REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering this application.

Disposition of Claims

Claims 1-3 and 5-12 are pending in the present application. Claims 1 and 7 are independent. The remaining claims depend, directly or indirectly, from claims 1 and 7.

Claim Amendments

Independent claim 1 has been amended by way of this reply to provide proper antecedent basis for the limitation "the power supply". No new matter has been added by way of these amendments. Applicant believes the included amendments do not require a new search, or at least simplify issues for appeal, and accordingly, Applicant respectfully requests entry and favorable consideration thereof.

Rejection(s) under 35 U.S.C § 112

Claims 1-3, 5, and 6 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Independent claim 1 has been amended in this reply in view of this rejection. Specifically, independent claim 1 has been amended to provide sufficient antecedent basis for the limitation "the power supply" in line 7. Thus, claim 1 now has proper antecedent basis for this claim limitation and is not indefinite. Accordingly, withdrawal of the rejection is respectfully requested.

Rejection(s) under 35 U.S.C § 103

Claims 1-3 and 5-12 were rejected under 35 U.S.C. § 103 as being obvious over U.S. Patent No. 5,172,330 issued to Watanabe *et al.* (hereinafter "Watanabe") in view of over U.S.

Patent No. 6,025,616 issued to Nguyen *et al.* (hereinafter "Nguyen"). For the reasons set forth below, this rejection is respectfully traversed.

The present invention is directed to a method and apparatus for reducing clock skew and noise on a computer chip by isolating power distribution between a clock tree and chip logic. As seen with respect to the exemplary embodiment of the present invention shown in Figure 4 of the present invention, a computer chip (60) has a clock tree (62) and chip logic (64). The clock tree has a clock generator (66) and a plurality of clock drivers (*e.g.*, 68, 70). The chip logic (64) has a plurality of logic elements (*e.g.*, 76, 78). A chip package (100) distributes power from a power supply (94) to the clock tree (62) and the chip logic (64) via separate leads (96, 98) (*see* Abstract, paragraph [0016]).

Accordingly, independent claim 1 of the present invention requires that power distributed from a power supply to the clock tree be isolated *in the chip package* from power distributed from the power supply to the chip logic. Claim 7 requires that the current drawn from the power supply for the chip logic operations be isolated in the chip package from the current drawn from the power supply for the clock tree operations.

Watanabe, in contrast to the present invention, fails to teach or suggest the limitations discussed above of the present invention. Watanabe is directed to the design of an integrated circuit in which the layout of the clock supplying circuit can be designed before the completion of the layout designing of the logic circuit area (*see* Watanabe, Abstract). Watanabe is concerned with separating power source lines (1201) for a logic circuit area (124) from power source lines (1202) for a clock buffer (1205) on an integrated circuit substrate. For example, as discussed with reference to Figure 12 of Watanabe, Watanabe states that as the power source lines (1201) and the power source lines (1202) are not connected with each other on the integrated circuit substrate (125), noise on power source lines (1202) caused by the clock buffer

(1205) is not transferred to the power source lines (1201) for the logic circuit area (124). Similarly, noise on the power source lines (1201) caused in the logic circuit area (124) does not influence the operation of the clock buffer (1205) (*see* Watanabe, col. 4, lines 23-45).

However, Watanabe does not contemplate a housing when designing the layout of the integrated circuit. Accordingly, Watanabe cannot teach that power distributed from a power supply to the clock tree be isolated in the chip package from power distributed from the power supply to the chip logic, as required by independent claim 1. Further, Watanabe cannot teach that current drawn from the power supply for the chip logic operations be isolated in the chip package from the current drawn from the power supply for the clock tree operations, as required by independent claim 7.

Nguyen, like Watanabe discussed above, fails to teach or suggest the limitations of the invention discussed above. Nguyen is directed to an electrical distribution system for gate arrays exposed to radiation environments (*see* Nguyen, col. 1, lines 6-10). Nguyen states that power and ground may be brought to chip (2) through conductors located within package (8) (*see* Nguyen, col. 1, line 62 – col. 2, line 4). However, Nguyen, like Watanabe, is completely silent with respect to power that is distributed from a power supply to the clock tree being isolated *in the chip package* from power distributed from the power supply to the chip logic.

As acknowledged by the Examiner and discussed above, Watanabe does not teach an apparatus including a chip package. Accordingly, Watanabe cannot teach that power distributed from a power supply to the clock tree is isolated *in the chip package* from power distributed from the power supply to the chip logic. Similarly, although Nguyen teaches that the chip (2) is typically housed in a package (8), Nguyen is completely silent regarding the separation of a clock tree power supply and a chip logic power supply *in the chip package*. Watanabe provides no motivation, and the Applicant knows of none, as to why one skilled in the art would seek the

teachings of Nguyen in light of Watanabe in regard to isolating a power supply to the clock tree *in the chip package* from power distributed from the power supply to the chip logic. In other words, it is abundantly clear that one skilled in the art would not turn from Watanabe, which in no way suggests a chip package or power supply isolation in the chip package, to Nguyen. Without the present application as a guide, one skilled in the art would find no motivation or suggestion in Watanabe to modify Nguyen to arrive at the limitations of the claimed invention. See *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (emphasis added).

Applicant further notes that the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990) (emphasis added). Further, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must *both* be found in the prior art, *not* in the Applicant's disclosure. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (emphasis added).

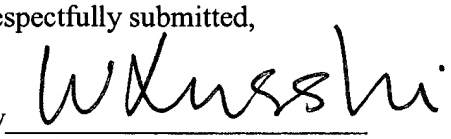
In view of the above, (i) Watanabe and Nguyen, whether taken separately or in combination, fail to show or suggest the present invention as recited in independent claims 1 and 7 and (ii) the combination of Watanabe and Nguyen is improper. Thus, independent claims 1 and 7 are patentable over Watanabe and Nguyen. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places the present application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226/114001; P6325).

Dated: April 20, 2005

Respectfully submitted,

By 

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